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10/675,745	09/30/2003	Manu Gulati	BP3252	8011

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EXAMINER	
CHU, WUTCHUNG	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,745	GULATI ET AL.	
	Examiner	Art Unit	
	Wutchung Chu	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8,9,11,12,14,15 and 17-29* is/are rejected.

7)☒ Claim(s) *3, 4, 7, 13, and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for domestic priority under 35 U.S. C. 119(e) is acknowledged.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claim 12 is objected to because of the following informalities:

Regarding claim 12, the claim is objected because the claim depends on itself.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 5, 6, 8, 9, 11, 12, 14,15, and 17-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hullett et al. (5689499).

Regarding claim 1, Hullett et al. discloses a method and apparatus for managing the statistical multiplexing of data in digital communication networks **(see column 3 line 35-37)** comprising:

receiving a data block at a receiver of the host device **(see figure7 arrow 48 and column 8 line16)**;

storing the data block in a receiver buffer **(see figure 8 arrow 66 and column 9 line 1-2 buffer for storing cells arriving on an input coupled to interconnection)**;

determining an input virtual channel corresponding to the data block **(see figure 2 VPI and VCI and column 6 line 33-37)**;

updating an input virtual channel linked list corresponding to the input virtual channel to include the data block **(see figure 12 box 254 cell start arrives and column 12 line 29-30)**;

determining an output virtual channel for the data block **(see column 7 line 24-32)**;

transferring the data block from the input virtual channel linked list of the receiver buffer to a destination within the host device via the output virtual channel **(see figure 12 box 250-258 and column 12 line 13-31)**; and

updating the input virtual channel linked list to remove the data block **(see figure 9 box 128 and column 10 line 7-16)**.

Regarding claim 2, Hullett et al. teaches determining an output virtual channel for the data block includes processing one or more of the input virtual channel **(see column 7 line 29-31)**, a header corresponding to the data block, a protocol corresponding to the data block, source identifier/address corresponding to the data block, and a destination identifier/address corresponding to the data block **(see column 7 line 10-31 and figure 4)**.

Regarding claim 5, Hullett et al. teaches comprising writing a data block to the receiver buffer and reading a data block from the receiver buffer in a single read/write cycle **(see column 11 line 31-37 and column 12 line 13-39)**.

Regarding claim 6, Hullett et al. teaches further comprising anticipating the write of a data block to the receiver buffer in a subsequent read/write cycle by reading a new free linked list head address from the receiver buffer at an old free linked list head address in a current read/write cycle **(see figure 12 and column 12 line 13-39)**.

Regarding claim 8, Hullett et al. teaches further comprising supporting a plurality of input virtual channel linked lists, wherein each input virtual channel linked list corresponds to a respective input virtual channel **(see figure 7 arrow 48 and column 9 line 40-52)**.

Regarding claim 9, Hullett et al. teaches further comprising supporting a free linked list that includes a plurality of vacant data blocks of the receiver buffer **(see column12 line 32-34)**.

Regarding claim 11, Hullett et al. teaches a method for routing data within a host device comprising:

- receiving a data block at a receiver of the host device, the data block received via an input virtual channel **(see figure7 arrow 48 and column 8 line16)**;

- storing the data block in a receiver buffer **(see figure 8 arrow 66 and column 9 line 1-2 buffer for storing cells arriving on an input coupled to interconnection)**;

- when the input virtual channel has identified therewith an output virtual channel **(see column 7 line 24-32)** updating an output virtual channel linked list corresponding to the output virtual channel to include the data block **(see figure 12 box 254 cell start arrives and column 12 line 29-30)**; and

- when the input virtual channel has not identified therewith an output virtual channel **(see figure9 arrow 100 and 104 and column 9 lines 35-41)**:

    - updating an input virtual channel linked list corresponding to the input virtual channel to include the data block **(see figure 9 box 128 and column 10 line 7-16 and see figure 9 arrow 100 and 102 and figure 8 box 68 admission & write controller and column 9 lines 34-39)**;

    - processing the data block to determine an output virtual channel for the data block **(see column 7 line 24-32)**;

    - updating an output virtual channel linked list corresponding to the output virtual channel to include the data block **(see figure 12 box 266 read out cell form buffer at C_addr and column 12 line 13-30)**; and

- updating the input virtual channel linked list to remove the data block **(see figure 12 box 264 remove first entry from link list and column 12 line 29-30)**.

Regarding claim 12, Hullett et al. teaches further comprising: transferring the data block from the receiver buffer to a destination within the host device based upon a corresponding output virtual channel **(see column 7 line 24-32)**; and updating the output virtual channel linked list to remove the data block **(see figure 12 box 266 read out cell form buffer at C_addr and column 12 line 13-30)**.

Regarding claims 14-15, 17, and 19 Hullett et al. teaches input buffer **(see column 9 line 1-2)** disclose all the limitations as discussed in the rejection of claims 5, 6, 8, and 9 and are therefore claims 14-15, 17, and 19 are rejected using the same rationales.

Regarding claim 18, Hullett et al. teaches further comprising supporting a plurality of output virtual channel linked lists, wherein each output virtual channel linked list corresponds to a respective output virtual channel **(see column 10 line 52-60)**.

Regarding claim 20, Hullett et al. teaches a received data processing and storage system comprising:

- an input that receives data blocks corresponding to a plurality of input virtual channels **(see figure 1 arrow 48)**;

- a routing module that determines an output virtual channel for data blocks based upon their respective input virtual channels **(see column 7 line 24-32)**;

- a receiver buffer operable to instantiate an input virtual channel linked list for storing data blocks on an input virtual channel basis and to instantiate a free list that identifies free data locations **(see column 9 line 1-10)**;

- a linked list control module operably coupled to the receiver buffer **(see column 10 line 18 and figure 8 box 68 Admission & Write Controller)**;

- input virtual channel linked list registers operably coupled to the linked list control module **(see column 10 line 21 modus operandi)**; and

- free linked list registers operably coupled to the linked list control module **(see column 10 line 66)**.

Regarding claim 21, Hullett et al. teaches further comprising an output that transmits data blocks corresponding to a plurality of input virtual channels **(see column 7 line 24-32 and figure 7 arrow 62)**.

Regarding claim 22, Hullett et al. teaches wherein:

- the receiver buffer **(see column 9 line 1-2)** is further operable to instantiate an output virtual channel linked list for storing data blocks on an output virtual channel basis **(see column 10 line 53 – column 11 line 2)**; and

- the system further comprises output virtual channel linked list registers **(see column 10 line 66)** operably coupled to the linked list control module and an input virtual channel to output virtual channel map **(see column 7 line 24-32)**.

Regarding claim 23, Hullett et al. teaches the receiver buffer comprises:

a pointer memory **(see column 10 line 66)**; and

a data memory **(see column 9 line 1-2)**, wherein a single address addresses corresponding locations of the pointer memory and of the data memory **(see column 10 line 17-26 and 28-34)**.

Regarding claim 24, Hullett et al. teaches the receiver buffer further comprises a packet status memory, wherein a single address addresses corresponding locations of the pointer memory **(see column10 line 18-33)**, the data memory, and the packet status memory **(see column 9 line 16-52)**.

Regarding claim 25, Hullett et al. teaches further comprising a pointer memory read port **(see figure 8 arrow 86)**, a pointer memory write port **(see figure 8 arrow 84)**, a data memory read port **(see figure 8 arrow 187)**, and a data memory write port **(see figure 8 arrow 177)**, each of which can access the receiver buffer in a common read/write cycle **(see figure 8)**.

Regarding claim 26, Hullett et al. teaches wherein:

a single pointer memory location can be read from and written to in a common read/write cycle **(see figure 8 box 68)**; and

- a single data memory location can be read from and written to in a common read/write cycle **(see figure 8 box 66 Buffer)**.

Regarding claim 27, Hullett et al. teaches wherein the receiver buffer comprises:

- a pointer memory **(see figure 8 box 68 Buffer)**;
- a data memory **(see figure 8 box 66 Buffer)**;
- a packet status memory **(see figure 8 box 66 Buffer and column 9 line 20-25)**; and
- wherein a single address addresses corresponding locations of the pointer memory **(see figure 8 box 68 Buffer)**, the data memory **(see figure 8 box 66 Buffer)**, and the packet status memory **(see figure 8 box 66 Buffer and column 9 line 20-25)**.

Regarding claim 28, Hullett et al. teaches further comprising:

- a pointer memory read port **(see figure 8 arrow 86)**;
- a pointer memory write port **(see figure 8 arrow 84)**;
- a data memory read port **(see figure 8 arrow 187)**;
- a data memory write port **(see figure 8 arrow 177)**;

- a packet status memory read port **(see figure 8 arrow 187)**; and

- a packet status memory write port **(see figure 8 arrow 177)**.

Regarding claim 29, Hullett et al. teaches wherein:

- a single pointer memory location can be read from and written to in a common read/write cycle **(see figure 8 box 68)**;

- a single data memory location can be read from and written to in a common read/write cycle **(see figure 8 box 66 Buffer)**; and

- a single packet status memory location can be read from and written to in a common read/write cycle **(see figure 8 box 66 Buffer and column 9 line 20-25)**.

Claim Rejections - 35 USC § 103

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hullett et al. in view of Gupta et al. (5555244).

Regarding claim 10, Hullett et al. disclose all the subject matter of the claimed invention with the exception of maintaining a mapping indicating a relationship between a plurality of input virtual channels and a plurality of output virtual channels.

Gupta et al. from the same or similar fields of endeavor teaches the use of protocol conversion **(see Gupta et al. column 29 line 9-15)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the protocol conversion as taught by Gupta et al. in the apparatus for managing the statistical multiplexing of data in digital communication networks of Hullett et al. in order to expand service offerings and interactive application support **(see Gupta et al. column line 11-34)**.

Allowable Subject Matter

9. Claims 3, 4, 7, 13, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hedds et al. (5432908) discloses high speed buffer management of share memory using linked lists and plural buffer managers for processing multiple requests concurrently.

Traw et al. (5274768) discloses high performance host interface for atm networks.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wutchung Chu whose telephone number is 571 270 1411. The examiner can normally be reached on Monday - Friday 1000 - 1500EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on 571 272 7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WC/
Wutchung Chu

5/22/07
WING CHAN
SUPERVISORY PATENT EXAMINER